ABSTRACT OF THE DISCLOSURE

A buffer amplifier architecture for buffering signals which are supplied in parallel to identical chips, particularly DRAM chips, on a semiconductor memory module, is disclosed. The architecture has adjustable delay circuits in each signal line and a delay detector circuit which receives a clock signal from the buffer amplifier architecture at the input and at the output of the buffer amplifier architecture, and takes the phase difference between the two signals to produce a control signal for setting the variable delay time of the delay circuits. To ensure that the delay time set by the delay detector circuit is independent of variations in parameters of the DRAM memory chips, the feedback path routed to the input of the delay detector circuit has a reference line network of the same structure and having the same electrical properties as capacitance elements which terminate the line network routed to the DRAM memory chips and the reference line network, and which have the same capacitances as the signal inputs on the DRAM memory chips .